Claims

1. A signal amplifier comprising:

at least two capacitive elements configured to retain a charge;

an interconnection of active devices between the at least two capacitive elements configured to operate upon a transient charge flow as a current when in operation, wherein the charge flow is partitioned into at least two parts according to a controlling parameter.

2. A signal amplifier according to Claim 1 wherein the at least two active elements are three terminal devices.

3. A signal amplifier according to Claim 1 wherein the at least two active elements are three terminal devices configured as long tailed pairs, each having a commonly connected terminal, wherein the transient charge flow enters the commonly connected terminals, and the signal amplifier further comprising a partition defined by the total charge sent to each output terminal and the controlling parameter is the input voltage difference.

4. A signal amplifier according to Claim 3, wherein the three terminal devices are MOSFET devices, wherein the commonly connected terminals are the source terminals of the devices, wherein the partition is the total charge sent to the separate drain terminals and wherein the controlling parameter is the voltage difference between the gate connections.

5. A signal amplifier according to Claim 3 further comprising a first capacitor and at least two secondary capacitors, wherein the long tailed pair is configured to partition a charge that transiently flows between the first capacitor and the two secondary capacitors such that, upon cessation of the transient current, an output voltage difference is expressed between the two secondary capacitors that is a representation of the input voltage between the two gate connections.

6. A signal amplifier according to Claim 3 wherein the output voltage is an amplified version of the input voltage.

7. A current mode switched capacitor comprising:

a long tailed pair of transistors, each having one terminal connected to a common voltage source and each connected in common by another terminal;

a cascode device connected at one terminal to the connected terminals of the long tailed pair;

a switched capacitor circuit connected on one end to another terminal of the cascode device and at another end to ground, and where the gate of the cascode device is connected to a bias voltage source, the switched capacitor circuit having a capacitor connected at one terminal to the source of the cascode device, and a switch connected at one terminal to the cascode device, another terminal connected to one end of a grounded current source, and yet another terminal connected to the common voltage source.

8. A method of amplifying a signal, comprising:

receiving an input signal;

opening a switch to cause the current from a current source to flow through the long tailed pair via the cascode device until the voltage in the capacitor drops;

cutting off the current source in response to the voltage in the capacitor dropping; and

closing the switch to cause the capacitor to charge up to the reference voltage.

9. A circuit, comprising:

a load circuit configured to generate a load current in response to an input signal;

an improved switched capacitor circuit configured to, wherein the switched capacitor includes a connection charge transferring circuit configured to utilize the charge transiently entering or leaving the switched capacitor circuit as an output parameter, retain this charge after a charge transfer, wherein the partitioning of the charge may have depended on an auxiliary input parameter.

10. A circuit according to Claim 3, further comprising a long tailed pair, wherein the auxiliary input parameter is the difference in input gate voltages.

11. A circuit comprising:

a long tailed pair input circuit configured to operate over a finite time interval over which a specified current flows such that a prescribed finite charge has passed at the end of this time interval, the circuit being configured to assess the total charge that has been partitioned as an output parameter during a finite time interval.